REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Status of Claims

Claims 1 – 20 are currently pending in the present application.

II. Amendments to the Claims

Claims 1, 11, and 18 have been amended to correct minor informalities. No new matter has been added by way of these amendments.

III. Drawings

As shown in the enclosed Replacement Sheet, Figure 2 has been amended to correct the informalities indicated in the form PTO-948 attached with the instant Office Action.

IV. Rejections Under 35 U.S.C § 112

§ 112, first paragraph

Claims 1 – 20 of the present application were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. For the reasons set forth below, this rejection is respectfully traversed.

As an initial matter in the traversal of the Examiner's rejections, Applicant notes that there is no requirement that there be a one-to-one correspondence between certain words in the Specification and in the claims for purposes of meeting the written description

requirement. Instead, to satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. *See, e.g., Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1319 (Fed. Cir. 2003); MPEP § 2163. As shown below, the Examiner unreasonably places dispositive emphasis on the correspondence between words in the Specification and in the claims instead of considering the Specification as would be read in whole by one skilled in the art.

"architectural analysis"

The Examiner maintains that the limitation "to perform an architectural analysis of the microprocessor" in independent claims 1, 11, 14, and 18 is not described in the present application. *See* instant Office Action, page 3. The Examiner supports this position by showing that the term "architectural analysis" appears only once in the present application. *See id.*

It is abundantly clear that the present invention discloses providing a visual representation of microprocessor events for the purpose of "architectural analysis." Those skilled in the art will readily and clearly recognize that an "architecture" of a microprocessor refers to the design of the microprocessor. The suggestion that "architectural analysis" was not contemplated by Applicant possibly renders the act of visually representing microprocessor events useless.

As clearly provided for in the present application, a visual representation of microprocessor events allows a user to analyze the design of the microprocessor:

> . . . In one or more embodiments, the present invention is a user-friendly tool that aids in the analysis of microprocessor performance characteristics. The present invention provides a visual representation of microprocessor events. This visual representation allows errors and trends to be easily detected and analyzed.

See Specification, paragraph [0037]; *see also, e.g.*, Specification, paragraph [0021] ("The present invention addresses the visualization of microprocessor internal resource utilization and correlation to instruction flow for the purpose of performance analysis and functional verification."); Specification, paragraph [0032] (". . . once the system graphically displays the execution behavior of a set of instructions, a user is given the ability to selectively view the data, e.g., highlight by time and instruction, zoom in and out, etc."). It is clear from the foregoing disclosure that Applicant contemplated and was in possession of the act of "architectural analysis" using a visual representation of microprocessor events.

Accordingly, because the disclosure of the present application clearly conveys that Applicant was in possession of the claimed limitation relating to "architectural analysis," withdrawal of the corresponding § 112, first paragraph, rejections is respectfully requested.

"optimizing"

The Examiner maintains that the limitation "optimizing a microprocessor design based on the architectural analysis" in independent claims 1, 11, 14, and 18 is not described in the present application. *See* instant Office Action, page 3. The Examiner supports this position by showing that the term "optimizing" appears only once in the present application. *See id.*, at page 4.

The present application clearly states that "the design can be optimized by selectively modifying the original design in view of the performing characteristics." *See* Specification, paragraph [0006]. While the Examiner labels this disclosure as a "nominal recitation" (*see* instant Office Action, page 4), it would be clear to those skilled in the art, especially in view of the cited disclosure in the "architectural analysis" traversal above, that Applicant clearly contemplated "optimizing" a design of a microprocessor based on analysis of a visual

representation of microprocessor events. Otherwise, there seems to be no need for any visual representation of microprocessor events or architectural analysis thereof if a designer cannot address design issues that would be discernible in such a visual representation.

Accordingly, because the disclosure of the present application clearly conveys that Applicant was in possession of the claimed limitation relating to "optimizing," withdrawal of the corresponding § 112, first paragraph, rejections is respectfully requested.

"execution behavior"

The Examiner maintains that the limitation "an execution behavior of instructions" in independent claims 1, 11, 14, and 18 is not described in the present application. *See* instant Office Action, pages 4 – 5.

The present application clearly conveys that "execution behavior" of instructions relates to internal state information resulting from execution of instructions. *See, e.g.*, Specification, paragraph [0022] (". . . the system modules may use *internal state information* from a separate microprocessor simulator, or may simulate *internal state information*, to display the *execution behavior* of the instructions.") (emphasis added); Specification, paragraph [0028] (". . . the system executes the set of instructions (step 46) and monitors *internal state information* of the microprocessor during the execution (step 48). The system uses the *internal state information* of the microprocessor to determine an *execution behavior* for the set of instructions.") (emphasis added); Specification, paragraph [0029] (". . . the present invention may use an external microprocessor simulator to obtain the *internal state information* required to display an *execution behavior* of a set of instructions.") (emphasis added); Specification, paragraph [0031] ("When the system receives the results of the simulation (step 70), the *internal state information* of the microprocessor design is determined (step 72). The system then uses the *internal state information* to graphically

display an *execution behavior* for the instructions (step 74).") (emphasis added); Specification, paragraph [0032] ("The system then simulates the execution of the instructions on a microprocessor (step 82) and generates *internal state information* representing the operation of the microprocessor (step 84). The system uses the *internal state information* to graphically display an *execution behavior* of the instructions (step 86).") (emphasis added). Moreover, noting that the original claims form part of the original disclosure and provide their own written description (*see In re Anderson*, 471 F.2d 1237 (C.C.P.A. 1973); MPEP § 2163), the disclosure of "execution behavior" is clear. *See* Specification, claim 1 as originally filed (". . . graphically displaying an *execution behavior* of the instructions on the microprocessor based on the *internal state information*") (emphasis added).

Accordingly, because the disclosure of the present application clearly conveys that Applicant was in possession of the claimed limitation relating to "execution behavior," withdrawal of the corresponding § 112, first paragraph, rejections is respectfully requested.

§ 112, second paragraph

Claims 1 – 20 of the present application were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. For the reasons set forth below, this rejection is respectfully traversed.

As discussed above, the meaning of the term "execution behavior" is clear in view of the present application. As shown in the above copious citation of disclosure in the present application, "execution behavior" clearly relates to internal state information of a processor resulting from execution of a set of instructions. Those skilled in the art will clearly recognize the scope of what constitutes state information in a microprocessor. Thus, the meaning of "execution behavior" is clear and definite. Accordingly, withdrawal of the § 112,

second paragraph, rejections is respectfully requested.

V. Rejections Under 35 U.S.C § 103

Claims 1 – 20 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,209,126 issued to Sasaki et al. (hereinafter "Sasaki") in view of U.S. Patent No. 6,490,716 issued to Gupta et al. (hereinafter "Gupta"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claims 1, 11, 14, and 18 of the present application require, in part, optimizing a microprocessor design based on architectural analysis of a visual representation of execution behavior of instructions. Although the portion of Gupta relied on by the Examiner generally discloses the concept of microprocessor design optimization, Gupta in no way discloses, or otherwise suggests, optimizing a microprocessor design based on architectural analysis of a visual representation of execution behavior of instructions, where the execution behavior relates to internal state information resulting from an execution of the instructions. In fact, Gupta actually "teaches away" from such "architectural analysis" because the technique disclosed in Gupta is automated:

> The invention relates to an automated method for designing a processor's control path. ***The method employs program routines implemented in software or hardware to automate the design of the control path based on the processor's instruction format and data path specification.*** It extracts parameters from a machine-readable description of the processor's instruction format specification, and generates a specification of the components in the control path.
>
> ***The method involves a number of unique process steps for automating the design of a processor's control path.***

See Gupta, column 2, lines 28 – 38 (emphasis added). Gupta's clear goal of automation stands in contrast to the claimed invention's requirement of performing an architectural analysis based on a visual representation. In other words, Gupta quite clearly "teaches away"

from the step of architectural analysis based on visual representation. Applicant notes that a prior art reference that "teaches away" from the claimed invention is a *significant* factor to be considered in determining obviousness. *See In re Gurley*, 27 F.3d 551, 554 (Fed. Cir. 1994) (emphasis added). Thus, like Sasaki, Gupta clearly fails to disclose optimizing a microprocessor design based on architectural analysis of a visual representation as required by independent claims 1, 11, 14, and 18 of the present application.

Further, in addition to the failure of Sasaki and Gupta to disclose each and every limitation of independent claims 1, 11, 14, and 18 of the present application, the Examiner has improperly combined the teachings of Sasaki and Gupta. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must a suggestion or motivation to combine the references within the prior art references themselves. In other words, regardless of whether prior art references can be combined, there must an indication within the prior art references *expressing desirability* to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). Further, ***the present application cannot be used a guide*** in reconstructing elements of prior art references to render the claimed invention obvious. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

Sasaki is generally directed to a pipeline stall detecting technique for reducing the labor and time needed to develop a source program. *See* Sasaki, Abstract. On the other hand, Gupta is directed to a technique for designing a processor's control path, where the control path specifies how instructions are fetched from memory, decoded, and dispatched to the control parts in a data path. *See* Gupta, Abstract; column 2, lines 3 – 5. There simply is no expression of desirability as required by *In re Mills* (cited above) in Sasaki to have any of the

recited features in Gupta. In fact, one presented with Sasaki would have no reason to turn to the teachings of a reference, such as Gupta, which is entirely not concerned with detecting pipeline stalls. Moreover, as there is no suggestion in Sasaki as to problems related to a processor's control path, it is completely unclear why one skilled in the art presented with Sasaki would have reason, based on the disclosure of Sasaki, to turn to the teachings of Gupta. Thus, just because Sasaki and Gupta both disclose techniques for designing an integrated circuit, such general overlap is not sufficient reason to combine these references, especially without any expressed desirability to do so. It is clear to one skilled in the art that Sasaki and Gupta are wholly unrelated as to their respective endeavors and there is no suggestion within either Sasaki or Gupta to incorporate, or otherwise combine, the teachings of one another.

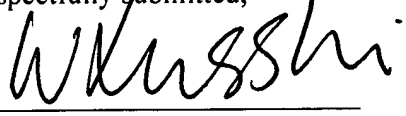
In view of the above, Sasaki and Gupta, whether considered separately or in combination, fail to disclose the present invention as claimed in independent claims 1, 11, 14, and 18 of the present application. Further, Sasaki and Gupta are not properly combinable under 35 U.S.C. § 103. Thus, independent claims 1, 11, 14, and 18 are patentable over Sasaki and Gupta. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of the § 103 rejection is respectfully traversed.

VI. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.016002; P4479).

Dated: November 30, 2005

Respectfully submitted,

By 

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IN THE DRAWINGS

Please amend Figure 2 as shown in the enclosed Replacement Sheet. Figure 2 has been amended to correct the informalities indicated in the form PTO-948 attached with the instant Office Action.